**IN THE SPECIFICATION**

Please amend the paragraphs as follows:

[00010] Fig. 3b is a schematic representation showing the contact pattern of Fig. ~~3b~~ 3a as having been patterned based on a predetermined contact pattern for the build up of the space transformer, according to an embodiment of the present invention;

[00019] According to an embodiment of the present invention, as will be described in further detail with respect to Figs. 1-6, a bare silicon wafer is provided, onto which vias are formed, for example using laser drilling techniques, in a pattern that matches the pad layout of the dies to be tested. Thereafter, a thin layer of an adhesion promoter, such as silicon oxide, is deposited onto the silicon wafer and into the vias. A layer of an electrically conductive material, such as copper, is then deposited on the layer of adhesion promoter, the thickness of the electrically conductive material being selected based on the deposition technology being employed, and being optimized for signal transfer. Then, the required contact pattern is defined, for example using standard photolithography techniques, and the build up of the space transformer is continued as required to ensure proper interconnect, power, ground and signal patterns depending on application needs. Thereafter the backside of the space transformer is removed, for example using a selective plasma etch process, to expose the electrically conductive material at the bottom of the vias. The space transformer may then be singulated from the ~~water~~ wafer and used in a test tool in a conventional manner.